IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

THE TRUSTEES OF PURDUE UNIVERSITY,

Plaintiff,

vs.

STMICROELECTRONICS N.V., ET AL.,

Defendant.

NO. 6:21–CV–727–ADA

JURY TRIAL DEMANDED

ST MICROELECTRONICS, INC.'S OPENING CLAIM CONSTRUCTION BRIEF

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EXHIBIT LIST

Ex. A: Declaration of Dr. Vivek Subramanian, PhD ("Subramanian Decl.")

Ex. B: U.S. Patent No. 8,035,112

Ex. C: U.S. Patent No. 7,498,633

Ex. D: James A. Cooper, et al., "Status and Prospects for SiC Power MOSFETs," in IEEE Transactions on Electron Devices, Vol. 49, No. 4, pp. 658–64 (Apr. 2002)

The Trustees of Purdue University (Purdue) asserts two patents—U.S. Patent Nos. 7,498,633 and 8,035,112—against Defendant STMicroelectronics, Inc. ("ST").[1] Both patents relate to metal oxide semiconductor field effect transistors (MOSFETS) with silicon carbide (SiC) substrates. The parties dispute four terms.

ARGUMENTS AND AUTHORITIES

A. '112 Patent

1. Technical Background

A field-effect transistor ("FET") is a type of transistor that uses an electric field to control the flow of current in a semiconductor. **Ex. A**: Subramanian Decl. ¶ 27. One type of FET is the MOSFET. In general, a MOSFET features at least five regions: the source, gate, drain, substrate, and gate insulator. *Id.* at ¶ 31. In such devices, current flows between source and drain regions under the control of a voltage applied to a gate electrode. **Ex. B**: U.S. Patent No. 8,035,112 (the '112 Patent) at 1:28–32. In Figure 3 of the '112 patent, the flow of current from the metal source contact layer 45, to sources 31, to drain 75 is depicted below. The source contact layer 45 is called a "source contact" because it makes electrical contact (connection) to the sources 31.

[1] Purdue also names as defendants STMicroelectronics N.V. ("STNV") and STMicroelectronics International N.V. ("ST Int'l"). STNV is not subject to the Court's jurisdiction, as detailed in its Motion to Dismiss [ECF 38], and ST Int'l has not yet been served in this case and therefore is not properly before the Court or subject to the Court's jurisdiction.

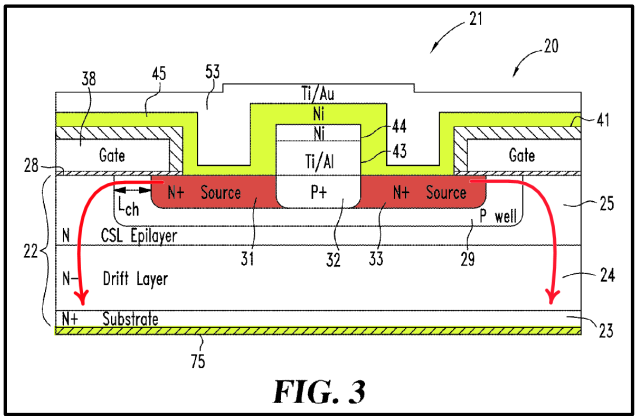

FIG. 3

(**Ex. B**: '112 Patent at Fig. 3, annotated)

[2]

Figure 1 of the '112 Patent (reproduced below) depicts a side, cross-sectional view of one cell region 10 of a so-called perfectly aligned, conventional DMOSFET. *Id.* at 3:25–26.

[2] *See, e.g.*, *id.* at 1:21–23 ("***This invention relates*** generally to semiconductor field effect transistors, and more ***particularly to field effect transistors having self-aligned source contacts***." (emphasis added)), 2:19–21 ("It is desired to produce DMOSFETs and related devices wherein misalignments of source contact and gate are reduced or eliminated."), 3:57–59 (describing problems that are "eliminated in the present invention by negating the opportunity for misalignment of source contact metal and gate"), 5:19–25 (referring to Figures 3 and 4, "the deposition of Ni metal contact 45 over the entire MOSFET 21 . . . makes conformal, direct and ***self-aligning contact*** with the Ti/Al and Ni metals 43 and 44 and, most importantly, with N- source implants 31 and 32." (emphasis added)), 6:63–7:2 ("Note that the area of the functional ***source contact is not determined by the alignment of any masking levels*** and is not subject to random misalignments during processing. Instead, it is totally determined by the spacing between adjacent polysilicon gates ***and is, in fact, self-aligned to the gate level***, being separated by the thickness of the oxide layer covering the gate." (emphasis added))

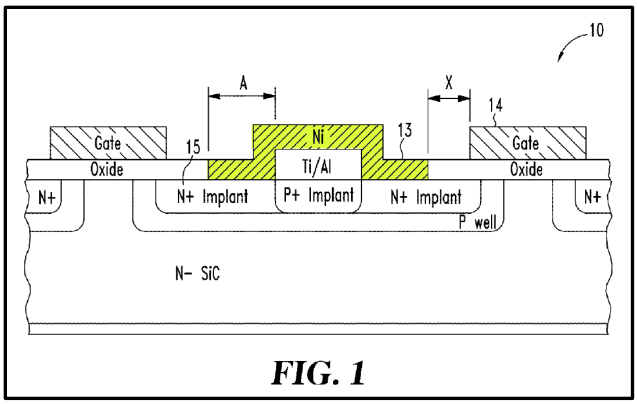

FIG. 1

(**Ex. B**: '112 Patent at Fig. 1, annotated)

Figure 2 shows an example of a MOSFET with a misaligned source contact 13' and P+ implant resulting from misalignment of masks. **Ex. B**: '112 Patent at 3:38–39. The Ni metal source contact 13' is misaligned to the right and the P+ implant 17' is misaligned to the left. *Id.* at 3:39–42.

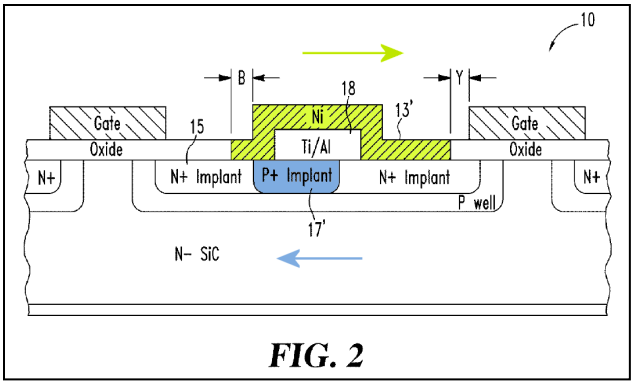

FIG. 2

The specification describes several problems caused by the mask misalignment. *See, e.g.*, *id.* at 3:42–57. These problems are purportedly "eliminated in the present invention [of the '112 Patent] by negating the opportunity for misalignment of source contact metal and gate." *Id.* at 3:55–59. Instead of using a mask to define the location of the source contact with respect to the gates with potential for misalignment, the invention provides for source contacts that are self-aligned to the gate level without using any masks. *Id.* at 2:24–26; 6:63–7:2. Part of the purported solution takes advantage of the fact that the MOSFET of the '112 Patent uses a silicon carbide (SiC) substrate rather than a conventional silicon substrate. When used with polysilicon gates, the silicon carbide substrate allows for silicon dioxide (also referred to simply as "oxide") to be formed, created, or grown over the gates at a faster rate than oxide on the substrate, and a source contact opening can then be formed through the oxide on the substrate without needing to use any mask. This process is further explained below in connection with Figures 3 and 5–8.

Figure 3 of the '112 Patent, shown below, depicts a side, cross-sectional view of the one cell region 20 of a DMOSFET in accordance with the present invention. *Id.* at 3:60–63. The device includes a substrate 23 and a number of layers and implants, collectively referred to as the substrate body 22. *Id.* at 4:8–11. Formed on top of the upper substrate surface 28 are gates 38 made of polysilicon. *Id.* at 4:66–5:2. The polysilicon gates 38 are surrounded along its top,

bottom, and sides by an insulating layer 41. *Id.* at 4:66–5:3. A contact metal 45 is formed over the entire MOSFET, covering the polysilicon gates 38 but insulated from each by the thick oxide layer 41 on the top and sides of the gate. *Id.* at 5:5–8.

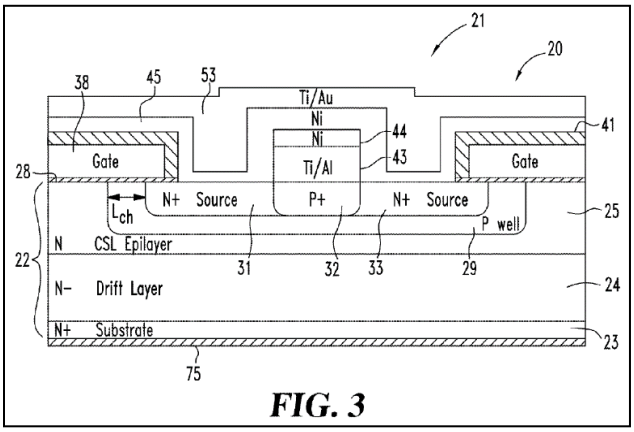

FIG. 3

Figures 5 through 8 of the patent show intermediate stages of fabrication of the DMOSFET and explain how the thicker oxide layer 41 on the top and sides of the polysilicon gate 38 is formed. Figure 5 shows substrate body 22 formed of SiC, and above the substrate body are a lower gate oxidation layer 59, a polysilicon layer 66, and a gate mask 62. *Id.* at 5:27–33. The gate mask 62 is used during an etching step to remove the portion of the polysilicon layer 66 that is not covered by the mask to create individual gates 38 (as revealed in Figure 6). *Id.* at 5:32–34.

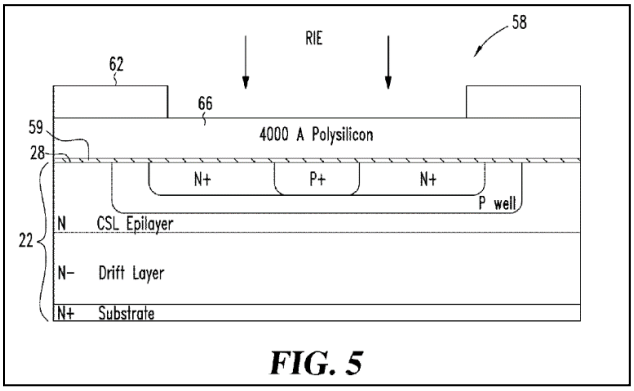

FIG. 5

As shown in Figure 6, etching removes portions of the polysilicon layer 66 within the mask outline that are not covered by the mask, down to the lower gate oxidation layer 59, thus leaving

only the polysilicon gates 38 at the locations under the gate masks, which protected those portions from etching. *Id.* at 5:54–60. At this stage, the intermediate semiconductor product contains a substrate body 22 made of *SiC* and individual patterned gates 38 made of *polysilicon*. This is significant because, as explained in the specification and more fully below, the invention of the '112 Patent takes advantage of the fact that polysilicon forms an oxide layer more rapidly than SiC does when both are thermally oxidized at certain temperatures. *Id.* at 5:61–65.

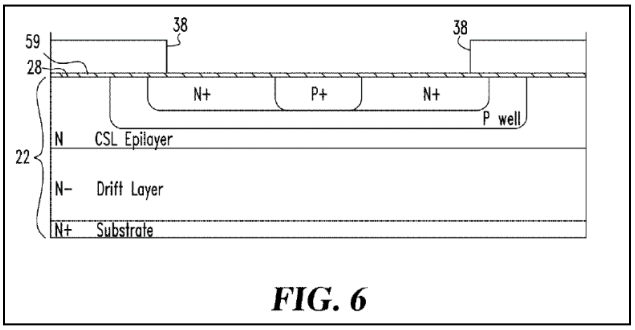

FIG. 6

(**Ex. B**: '112 Patent at Fig. 6)

In Figure 7, the intermediate semiconductor product is next thermally oxidized (by being exposed to heat and oxygen), so that an oxide is grown over the entire upper surface, including the gates and substrate body. *Id.* at 6:20–22.

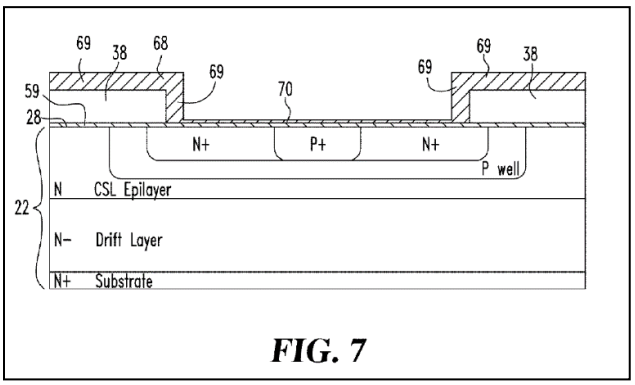

FIG. 7

(**Ex. B**: '112 Patent at Fig. 7)

Because of the different reactive properties of polysilicon and SiC, the oxidation grows roughly 10 or more times faster on the polysilicon gates 38 than on the SiC substrate. *Id.* at 6:27–30. This phenomenon results in (1) a thin oxide layer 70 grown over the upper surface 28 of the

SiC substrate and (2) a much thicker oxide layer 68 grown over the polysilicon gates 38.[3]

Finally, a short oxide etch is applied to the entire semiconductor product for the purpose of removing the thin oxide layer (59 and 70) over the SiC substrate. *Id.* at 5:65–6:1, 6:45–49. Because the oxide layers have different thicknesses, the short etch completely removes the thin oxide layer (59 and 70) over the SiC substrate while removing only a small amount of the oxide over the gates, thus still leaving a thick oxide layer 69 on the top and sides of each polysilicon gate 38 (as shown in Figure 8).[4] By removing the thin oxide layer (59 and 70) over the SiC substrate, the surface of the substrate is exposed in this area so the metal source contact can later be deposited and make electrical contact with this region.

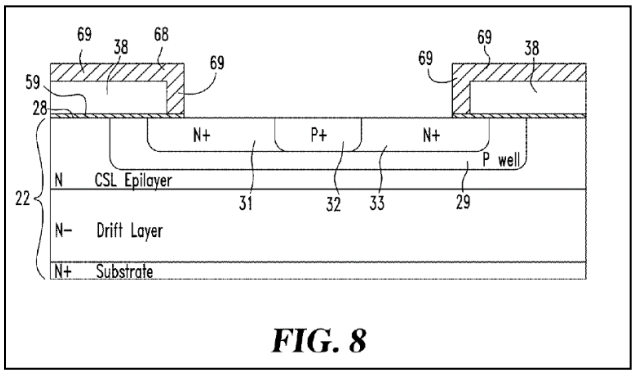

FIG. 8

(**Ex. B**: '112 Patent at Fig. 8)

If the oxide layer 69 that covers and insulates gates 38 was not able to be grown to be much thicker than the oxide layer over the substrate 22, then the previously discussed oxide etch could

[3] *Id.* at 6:31–34 ("The foregoing oxidation growing step *16d* grows oxidation on the polysilicon gates 38 about ten times faster or more than on the SiC substrate (on which there is already about a 50 nm oxidation layer 59). Consequently, oxidation layer 68 on top and on the sides of each gate 38 has grown to about 500 nm thick (at 69), while only about 10 nm or less of oxidation are added to upper substrate surface 28 (at 70).").

[4] *Id.* at 6:1–4 ("Because it is much thicker, the oxide over the polysilicon gate is not completely removed during this process and forms an insulating layer over and around the poly silicon gate 38."); *id.* at 6:45–50 ("A short oxide etch is then applied long enough to completely remove the thin oxide layer (comprising previously formed layers 59 and 70) over substrate surface 28 and between gates 38, which exposes N+ and P+ implants 31, 32 and 33 and thus still leaves a very thick insulating oxide layer 69 on the top and sides of gates 38.").

not be used to remove only the oxide over the substrate without also removing the insulating oxide layer 69. That would be the case with a so-called "deposited" type of oxide. **Ex. A**: Subramanian Decl. ¶ 69. In a deposited oxide, for example in the case of silicon oxide, chemicals containing silicon and oxygen are mixed together in a chamber and combine to form a layer of silicon oxide that deposits onto the surface of the wafer, covering the wafer with a uniform thickness of oxide regardless of the underlying material (e.g., SiC versus polysilicon). *Id*. at ¶¶ 69–70, 79, 81–82. In that case, a mask would need to be carefully aligned to define the areas where oxide should and shouldn't be removed by etching (like that shown in Fig. 5 for etching the polysilicon to form the gates), which as mentioned above, presents an opportunity for mask misalignment. *Id*. But the invention purportedly eliminates this issue by providing for a thick oxide layer to be formed, created, or grown exactly where it is needed (surrounding the polysilicon gates) and then preserving that thick layer without having to worry about the mask alignment errors of conventional processing techniques. This is what the '112 Patent refers to as forming a source contact that is "self-aligned to the gate level" *See id*. at ¶¶ 56, 64; **Ex. B**: '112 Patent at 6:63–7:2.

2. Disputed Terms

a. "a second, thicker oxide layer" (claim 1) and "a gate oxide layer" (claim 6)

Term	Purdue's Proposed Construction	ST's Proposed Construction
"a second, thicker oxide layer" (claim 1)	"layer of oxide that is on the tops and sides of each gate and that is thicker than the layer of oxide below each gate"	"an oxidation layer formed, created, or grown by reacting the gate, thicker than the first oxide layer"
"a gate oxide layer" (claim 6)	"layer of oxide that is on the tops and sides of each gate and that is thicker than the layer of oxide below each gate"	"an oxidation layer formed, created or grown by reacting the gate"

Claims 1 and 6 of the '112 Patent each require two oxide layers and it is the second of these oxide layers that is at issue for construction: (1) a first oxide layer on top of the substrate

and under the gates and (2) a second oxide layer that covers the top and sides of the gates:

Claim 1 (excerpted)	Claim 6 (excerpted)
1. A silicon carbide power MOSFET, comprising: . . . a first oxide layer between said first gate lower surface and said upper surface of said drift layer; a second, thicker oxide layer over said top surface and sidewall of said first gate; and	6. A MOSFET structure, comprising: . . . a substrate surface oxidation layer on said upper surface of said substrate body and adjacent said source region; . . . a gate oxide layer, thicker than said substrate surface oxidation layer, over said tops and sides of each of said gates; and . . . .

These first and second oxide layers are illustrated in Figure 3:

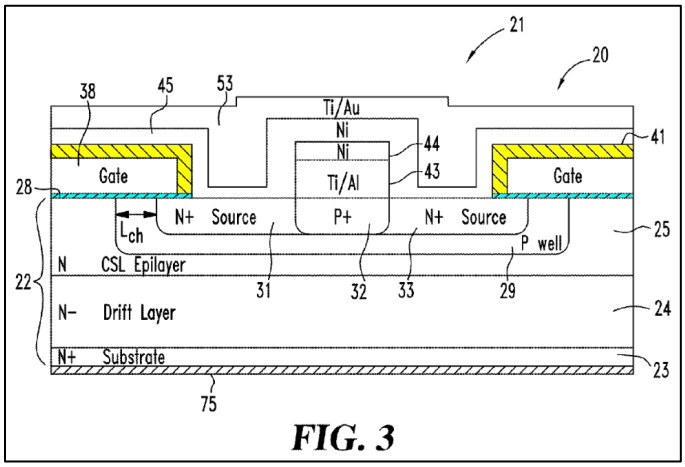

FIG. 3

(**Ex. B**: '112 Patent at Fig. 3, annotated)

Here, the disputed terms—"a second, thicker oxide layer" (claim 1) and "a gate oxide layer" (claim 6)—refer to the layer of oxide that is located over the top and sides of the gates (annotated in yellow in Figure 3 above). The parties' central dispute is whether this layer is limited to an oxidation layer of the type that is *formed, created, or grown* by reacting the gate, or whether it can include a *deposited* oxide. The patent is explicit on this point: ***the invention*** is limited to an oxide that is *formed, created, or grown* by reacting the gate. The specification states that the invention is to be broadly construed ***so long as*** the insulating oxidation layer around the gate is limited to one that is ***formed, created, or grown by reacting the gate***:

> ***Alternative embodiments are contemplated*** wherein the secondary steps (and even certain of the primary steps) can be performed in ways other than recited, with materials, solutions and concentrations other than recited, and for times and under temperatures and conditions other than recited, ***so long as the gate and substrate source (or other ohmic contact materials) react to form, create or grow an insulation layer (such as SiO_2)*** sufficiently faster, larger and/or with more insulating capacity at the gate surface than at the substrate surface and that will therefore be uniformly removable at a rate which will remove all such formed, created or grown layer substantially or entirely completely from the substrate surface and leave a sufficiently insulative layer around the gate.

Id. at 7:20–33 (emphasis added). The reason is that forming, creating, or growing the oxide layer around the gate (as opposed to using a deposited oxide layer and then creating an opening using a mask) is how the patent allegedly achieves "self-aligned source contacts," which is what the named inventors describe as their purported invention:

- Title: "SiC Power DMOSFET with ***Self-Aligned Source Contact***" (emphasis added)
- Background of the Invention: "***This invention relates*** generally to semiconductor field effect transistors, and more ***particularly to field effect transistors having self-aligned source contacts***." *Id.* at 1:21–23 (emphasis added).
- Summary of the Invention: "***The present invention provides*** high voltage power MOSFETs, with ***self-aligned source contacts*** and a method for making the same." *Id.* at 2:24–26 (emphasis added).
- Detailed Description: "the area of the functional ***source contact is not determined by the alignment of any masking levels*** and is not subject to random misalignments during processing. Instead, it is totally determined by the spacing between adjacent polysilicon gates ***and is, in fact, self-aligned to the gate level***, being separated by the thickness of the oxide layer covering the gate." *Id.* at 6:63–7:2 (emphasis added)).[5]

Statements such as these, directed to "the present invention" as a whole, are limiting. *See, e.g.*, *Regents of the Univ. of Minn. v. AGA Med. Corp.*, 717 F.3d 929, 936 (Fed. Cir. 2013) ("When a

[5] *See also, e.g.*, *id.* at 3:57–59 (describing problems that are "eliminated in the present invention by negating the opportunity for misalignment of source contact metal and gate"); *id.* at 5:19–25 (referring to Figures 3 and 4, "the deposition of Ni metal contact 45 over the entire MOSFET 21 . . . makes conformal, direct and ***self-aligning contact*** with the Ti/Al and Ni metals 43 and 44 and, most importantly, with N-source implants 31 and 32." (emphasis added)).

patent thus describes the features of the 'present invention' as a whole, this description limits the scope of the invention.").

As explained in the Technical Background section above, the whole point of the purported invention of the '112 Patent is that during the time it takes to form, create, or grow a thick oxide layer around the polysilicon gate, only a very thin oxide layer forms on the silicon carbide substrate. Thus, the thin oxide layer on the substrate can be removed with a short oxide etch (leaving the oxide over the gate) instead of a using a conventional step of etching with a mask.

Purdue's proposed constructions improperly broaden the claims' scope to cover the very oxide deposition and masking process the patent purports to obviate. **Ex. A**: Subramanian Decl. ¶¶ 58, 79–84. Purdue's proposed constructions should therefore be rejected. In contrast, ST's proposed constructions should be adopted because they track the invention disclosed in the specification and are the only interpretation that aligns with the stated purpose: to eliminate the need for a mask to position the source contact opening through the oxide, which can result in misalignment problems. *Id.* at ¶¶ 69–70, 79, 81–82.

B. '633 Patent

1. Technical Background

The '633 Patent is directed to semiconductor devices, such as MOSFETS, for high-voltage power applications. **Ex. C**: U.S. Patent No. 7,498,633 (the '633 Patent) at 1:12–14. Specifically, claim 9 of the '633 Patent is directed to a "double-implanted" MOSFET. Figure 1 of the '633 Patent shows a cross-section (i.e., a cut-away side view) of the claimed semiconductor device:

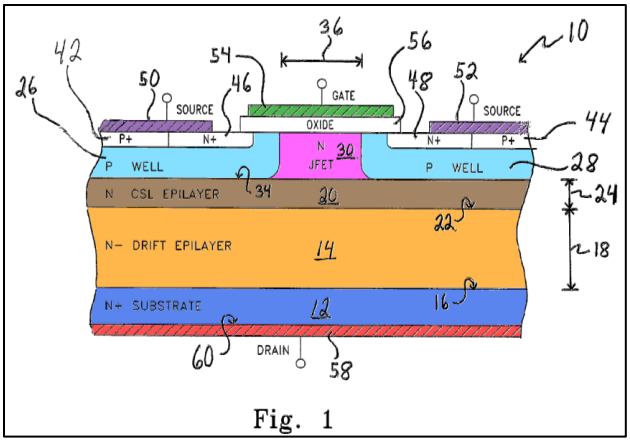

Fig. 1

(**Ex. C**: '633 Patent at Fig. 1, annotated)

As Figure 1 shows, the device includes the following elements (listed from bottom to top): **a drain 58** (*id.* at 7:17–19); **a substrate 12** that can be formed from silicon-carbide material and doped with N-type impurity to an "N+" concentration (*id.* at 4:4–13); **a drift layer 14** formed on a front side 16 of the substrate 12 (*id.* at 4:20–21, 4:35–41); **an optional current spreading layer 20** ("CSL") (*id.* at 2:59–66; 3:16–22); "**two doped semiconductor wells or base regions 26, 28**" that "are doped with a P-type impurity to a 'P' concentration" (*id.* at 5:23–24, 5:42–43); **a JFET region**, i.e., the region between the wells 26 and 28, where the JFET region 30 and the CSL 20 have similar doping concentrations (i.e., "N" concentration) (*id.* at 5:25–26, 5:54–56, 6:3–5); **source (metallic) electrodes 50, 52**. (*id.* at 7:4–6); and **a gate 54**. (*id.* at 7:13–15)

There can be many different configurations and design choices, but a FET generally includes at least a source, a drain, and a gate. **Ex. A**: Subramanian Decl. ¶ 31. Like the FET, a MOSFET has source, gate, and drain elements, but also includes a gate insulator. *Id.* As would be understood by a person of ordinary skill in the art (POSITA), the flow of current in such devices is controlled by applying a voltage to the gate (thereby creating an electric field), which in turn alters the conductivity of the channel formed under the gate and between the drain and the source. In the structure shown in Figure 1 (annotated below), the current moves from the source electrode, horizontally through the channel region, and then, upon entering the JFET region,

turns vertically down to the drain. Specifically, in Figure 1, when an appropriate voltage is applied to the gate (54), current is able to flow between the sources (50 & 52) and the drain (58), through the JFET region (30). *Id.* at ¶ 27. As a result, the device can be used as a switch, turning current flow on and off. *Id.*

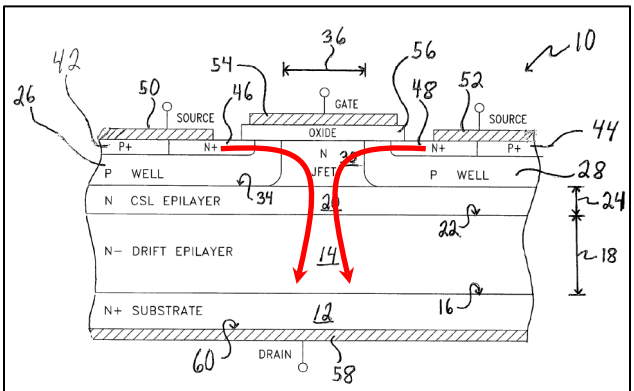

Fig. 1

(**Ex. C**: '633 Patent at Fig. 1, annotated)

2. Disputed Terms

a. The preamble of claim 9 is limiting.

Purdue's Proposed Construction	ST's Proposed Construction
The preamble of claim 9 is not limiting.	The preamble of claim 9 is limiting.

The "double-implanted metal-oxide semiconductor field-effect transistor" phrase in the preamble of claim 9 gives life, meaning, and vitality to the claim (which otherwise recites an incomplete MOSFET structure); is critical to understanding the claim's scope; and distinguishes the double-implanted device of claim 9 from the non-double-implanted devices of other claims.[6]

Claim 9 is reproduced below (emphasis added):

[6] A preamble is limiting if it recites essential structure or steps, or is "necessary to give life, meaning, and vitality" to a claim. *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002) (quoting *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305 (Fed. Cir. 1999)). A preamble is not limiting "where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention." *Id.* (quoting *Rowe v. Dror*, 112 F.3d 473, 478 (Fed. Cir. 1997)).

> 9. ***A double-implanted metal-oxide semiconductor field-effect transistor comprising***:
>
> a silicon-carbide substrate;
>
> a drift semiconductor layer formed on a front side of the semiconductor substrate;
>
> a first source region;
>
> a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis;
>
> a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode;
>
> a second source region;
>
> a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis;
>
> a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode; and
>
> a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.

First, without the preamble, claim 9 is structurally incomplete. For example, although the preamble indicates that claim 9 is directed to a type of MOSFET device, the claim body is missing essential MOSFET elements, including a gate, gate insulator, and drain. **Ex. A**: Subramanian Decl. ¶¶ 29–31. Inclusion of the preamble as a structural element helps fill in these vital missing pieces in the device configuration. *Id.* at ¶ 30.

Second, of the elements that *are* listed in the body of claim 9, the preamble contextualizes the possible arrangements and cooperation of those elements, particularly where the relative arrangement and cooperation of certain elements is entirely undefined. For example, the claim is silent regarding the position of the first and second source regions, and whether the source regions have any connection or cooperation with other claim elements. *Id.* at ¶ 33. The claim does not say whether the source regions are in, on, between, or even in contact with either the substrate or drift semiconductor layer. *Id.* By identifying the type of device as a double-

implanted MOSFET, however, the preamble provides necessary context regarding how the components must be arranged so as to result in a FET, rather than some other device. *Id.*

Third, the preamble of claim 9 fundamentally informs what type of semiconductor device is being claimed: a double-implanted MOSFET, as opposed to another type of transistor. The specification describes a number of embodiments, including a MOSFET, double-implanted MOSFET, and vertical double-implanted MOSFET. *See, e.g.*, **Ex. C**: '633 Patent at 1:40–2:26 (describing a MOSFET embodiment), 2:26–3:6 (describing a double-implanted MOSFET embodiment), 3:7–40 (describing a vertical double-implanted MOSFET embodiment). Without the preamble, even if a POSITA could conclude that the device of claim 9 is a MOSFET, a POSITA would not necessarily conclude that it is double-implanted. Indeed, the specification states that the patent's "MOSFET ***may be*** a double-implanted MOSFET (DMOSFET)," *id.* at 2: 26–27 (emphasis added), but that the device also "may be embodied as other types of MOSFET devices," *id.* at 4:6–11. Highlighting the issue even further, while all claims of the '633 Patent are directed to MOSFETs, other preambles (like claim 1's) do not include the "double-implanted" element. Thus, is it clear that the patentee meant to differentiate between a MOSFET and a *double-implanted* MOSFET, and limit claim 9 to a particular double-implanted embodiment in the specification. By specifying different embodiments in the preambles of claims 1 and 9, the patentee intended to identify the specific embodiments being claimed. Accordingly, a POSITA would understand the preamble to structurally distinguish the device at issue in claim 9 (a double-implanted MOSFET) from the device at issue in claim 1 (simply a MOSFET). **Ex. A**: Subramanian Decl. ¶¶ 34–35.

The patent's specification and other claims make clear that the "double-implanted metal-oxide semiconductor field-effect transistor" phrase is a necessary and defining aspect of claim 9, which was intended to cover only a specific type and configuration of semiconductor device. The

preamble should therefore be a limitation.

b. "less than about three micrometers" (claim 9)

Purdue's Proposed Construction	ST's Proposed Construction
"about three micrometers or less"[7]	Indefinite

Claim 9 is directed to a double-implanted MOSFET that includes, among other things, "a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers." The use of "less than about three micrometers" to describe the JFET width in this limitation renders the claim indefinite because a POSITA cannot determine the upper or lower limits of the numerical range.

Neither the claims nor the specification provide any design reasons for the "less than about three micrometers" high-end limit on the JFET region size. And a POSITA, understanding the design tradeoffs inherent in MOSFET devices, has no guidance regarding the criticality of the less than about 3-micrometer measurement to the invention in order to reasonably determine the upper limit of the range.[8] By way of analogy, using the Court's classic example of a "vertical pipe," it is as if we do not know whether the pipe needs to be "vertical" to (a) enable a floating dock to move up and down, where precision is likely not very important, or (b) launch a rocket to the moon, where precision is likely critically important. In this patent, it is not specified what characteristic the "less than about three micrometers" limitation is supposed to achieve, so a

[7] Underscoring this term's indefiniteness, Purdue's construction broadens the scope of the term to include the value "about 3" instead of encompassing only values "less than about 3," as the term requires. This would be like construing the phrase "less than 3" to mean "less than *or equal to* 3."

[8] Worse, there is no basis for reasonably determining the lower end of the "less than about three micrometers" range of JFET widths. At the lower end, the phrase would appear to literally include any dimension down to zero width. But the '633 Patent does not disclose how to make operable vertical DMOSFETs at all possible dimensions down to and including zero JFET width. **Ex. A**: Subramanian Decl. ¶ 43. And if the JFET was reduced to zero width, the device would no longer be a vertical double-diffused MOSFET. *Id.*

POSITA does not have context to understand how close the measurement can (or must) be to 3 micrometers to be acceptable. This is why the term is indefinite.

To begin with, the literal words "less than about three micrometers" do not express precise boundaries on the scope of the term regarding either the upper or lower limits of the JFET width. The term says only "less than about." Unremarkably, the phrase "less than" denotes that the claimed range must be *less than* the recited value. But when "less than" is modified by the word "about"—a term of approximation that permits wiggle room on either side of the recited value—the scope of the range becomes unclear. Take, for example, a JFET width of 3.5 micrometers. It is unclear whether this value falls inside or outside the scope of the claims. Is 3.6 "about 3" making 3.5 "less than about 3," or is 3.3 "about 3" making 3.5 outside the scope of this term? The answer depends on the precision required, but the '633 Patent provides no guidance on the issue of precision. So when competing experts disagree on the upper limit, there is nothing in the specification to help guide the Court or the jury to determine which one would be correct.

When "about" is used as part of a numeric range, "[its] meaning depends on the technological facts of the particular case."[9] The criticality of the numerical limitation to the invention determines how far beyond the claimed range the term "about" extends the claim.[10] In other words, here, we must look to the *purpose* that the "less than about three micrometers" limitation serves to determine with any reasonable certainty how much greater than 3 micrometers the JFET width can be and still serve that purpose. *See id.* at 1368 ("To be clear, it is the purpose of the *limitation* in the claimed invention—not the purpose of the invention

[9] *Cohesive Techs., Inc. v. Waters Corp.*, 543 F.3d 1351, 1368 (Fed. Cir. 2008) (alteration in original) (quoting *Pall Corp. v. Micron Separations, Inc.*, 66 F.3d 1211, 1217 (Fed. Cir. 1995)).

[10] *Id.* (citing *Ortho–McNeil Pharm., Inc. v. Caraco Pharm. Labs., Ltd.*, 476 F.3d 1321, 1327 (Fed. Cir. 2007)).

itself—that is relevant."). But as explained below, neither the specification of the '633 Patent nor a POSITA's knowledge of the subject matter at issue provides a basis for determining the scope of the phrase with reasonable certainty.

First, the specification does not describe the purpose that the "less than about three micrometers" high-end limit on JFET width is supposed to achieve in the claimed MOSFET device. For example, the '633 Patent does not say there is any particular characteristic or purpose of the device that is achieved with a JFET width in the vicinity of less than 3 micrometers that is not achievable at other dimensions—whether 3.1 micrometers, 3.5 micrometers, 4.0 micrometers, or any other dimension. To the contrary, the specification explains that there are multiple characteristics that a designer may consider: "One design consideration . . . is the blocking voltage of the semiconductor device. [F]or high-voltage power applications, a high blocking voltage is generally desirable. Another design consideration . . . is the specific on-resistance." **Ex. C**: '633 Patent at 1:18–28. Moreover, the specification explains that MOSFET design involves many parameters (including the width of the JFET region) that are interdependent, where design choices for one parameter invariably affect the other parameters:

> "[T]he design of the semiconductor device 10 involves a number of parameters that may affect or be interdependent upon each other. As such, the design process of the semiconductor device 10 may include a number of reiterative steps of selecting a width 36 and a doping concentration for the JFET region 30, selecting a doping concentration and a thickness for the current spreading layer 20, selecting a doping concentration and a thickness 18 for the drift layer 14, and/or selecting values for other parameters to achieve the desired characteristics of the semiconductor device 10."

Id. at 6:55–62. Accordingly, the specification concedes that selection of various design parameters (including JFET width) depends on "desired characteristics" of the MOSFET device, but fails to provide *any* characteristics motivating the selection or required precision of the 3-micrometer JFET measurement. As a result, there is no basis in the specification from which to

determine the criticality of the JFET width, the precision required, or the resulting range of values encompassed by the claim. **Ex. A**: Subramanian Decl. ¶ 44.

Second, the technical subject matter and knowledge of a POSITA provide no more certainty regarding the purpose for the "less than about three micrometers" JFET-width limitation or the acceptable boundaries of that range. A POSITA would understand that JFET widths in a silicon carbide power MOSFET could widely. *Id.* at ¶ 41. Further, this term has no explicit lower range (thus including zero μm). Yet a POSITA would understand that the JFET width must more than zero μm in order for a MOSFET to function. *Id.* at ¶ 43. Yet again, the specification provides no guidance on the lower limit either. Consistent with the specification, a POSITA would understand that the different selections of MOSFET parameters create design tradeoffs. *Id.* at ¶¶ 39, 43. For example, a 2002 paper co-authored by named inventor James Cooper explained the design tradeoffs involving JFET size and total device size:

> "In addition to the resistance of the MOS inversion layer, the specific resistance of the DMOSFET also includes the resistance of the JFET region between the implanted p-base regions. This introduces a tradeoff in the design: As the spacing between base regions is increased to reduce the JFET resistance, the area of the device also increases, increasing R_{SP}. In addition, as the spacing increases, and the effectiveness of the base regions in terminating the electric field in the blocking state diminishes, increasing the field in the oxide and lowering the blocking voltage."[11]

Although the patent confirms there are many parameters to trade off, neither the specification nor claim 9 dictate any particular combination of design parameters (such as thickness or doping concentrations for any layer) that would therefore influence or inform what is within the claimed range for the JFET width. **Ex. A**: Subramanian Decl. ¶ 42. Instead, the patent leaves the JFET width and other parameters to the subjective personal choice of the

[11] **Ex. D**: James A. Cooper, et al., "Status and Prospects for SiC Power MOSFETs," in IEEE Transactions on Electron Devices, Vol. 49, No. 4, pp. 658–64 (Apr. 2002), at p. 659.

designer. *Id.* Thus, because the desired characteristics of the semiconductor device are subjective and the particular JFET width depends on the designer's personal choice, there is no way for a POSITA reading the '633 Patent to know the boundaries of this claim element. *Id.*

Courts have found similar claim terms to be indefinite. For example, in *Amgen, Inc. v. Chugai Pharm. Co.*, the district court found a claim drawn to a protein having a "specific activity of at least about 160,000 IU" indefinite. 927 F.2d 1200, 1203 (Fed. Cir. 1991). The district court explained that "bioassays provide an imprecise form of measurement" and that use of the term "about," coupled with the range of error already inherent in the specific activity limitation, failed to inform others what specific values below 160,000 IU, if any, might constitute infringement. *Id*. at 1217. The Federal Circuit agreed, pointing out "that nothing in the specification, prosecution history, or prior art provides any indication as to what range of specific activity is covered by the term 'about.'" *Id*. at 1218.

Similarly, claims reciting "less than approximately" and "greater than approximately" were held indefinite in *Hamilton Products, Inc. v. O'Neill*, 492 F. Supp. 2d 1328, 1332–33 (M.D. Fla. 2007). Concluding that the specification and prosecution history shed little light on what the dimensions were intended to cover, the court held the terms to be "incapable of construction." *Id.* at 1337–40. In reaching its decision, the court found persuasive the following expert testimony:

> "[I]t is not illogical to conclude that . . . 'less than about' 0.8 yields a measurement of (1) any value less than but not including 0.8 because of the phrase 'less than' but without the phrase 'or equal to,' (2) any value less than or equal to 0.8 because of the phrase 'less than' and the word 'about,' and (3) any value less than more or less than 0.8, including values just 'greater than' 0.8 because a value greater than 0.8 gives import to the chosen word 'about' (or approximately)."

Id. at 1339; *see also Synthes (USA) v. Smith & Nephew, Inc.*, 547 F. Supp. 2d 436, 454 (E.D. Pa. 2008) (finding claims reciting "less than about 2%" to be indefinite on grounds similar to those in *Hamilton Products*). This Court should hold "less than about three micrometers" indefinite.

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CERTIFICATE OF SERVICE

I certify that on February 21, 2022, the foregoing document was served via electronic mail on counsel of record for Plaintiff.

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